Design Review 1, Los tOHMales Call$_e$ntes, VLSI 4332

Lauren Cash <lec2yy>
Chuhong Duan <cd8dz>
Rebecca Reed <rcr4dd>
Andrew Tyler <adt2bt>
ECE 4332/6332 – Fall 2012
University of Virginia

ABSTRACT
In this paper, we give an overview of our design for both a 1MB embedded low-power SRAM unit and a high-speed cache. The design presented in this paper is meant to give the PICo board an indication of the functionality of one block of our SRAM and provide appropriate simulations at the bit cell level to show the read, write and idle stages of the SRAM.

1. INTRODUCTION
Our team, Los tOHMales Call$_e$ntes, is attempting to design the most efficient embedded low-power SRAM unit possible. In order to achieve this we will submit a series of design reviews and proposals to the PICo board to attempt to convince them that our design is superior to any competing design. The rest of this document outlines our initial design and functionality. This design does not attempt to optimize area, power or delay, instead we hope to demonstrate the functionality of our memory unit and display initial simulation results to support the claim that our design works at the bit-cell level.

2. DESIGN
2.1 Block Design
Our team designed a block for our future 1MB SRAM unit capable of performing reads and writes at low power. This design follows the requirements outlined in the Design Review Document. Specifically, our SRAM block is made up of 64 rows, and 16 columns. Using decoders, these rows and columns get activated to read or write an 8 bit word. These operations rely on the logic located in the pre-charge component and the sense amps we have designed. During a read, the pre-charge pushes the bit lines for a designated column high and then floats the lines. This allows the selected bit cell to push its value out to the bit line which can then be read through the output mux of the block. The sense amp detects when the voltage of the bit lines falls below the desired threshold needed for a read, it will then trigger the pre-charge and the bit lines will be pushed back to VDD. The overall design is captured in the block diagram shown in Figure 1.

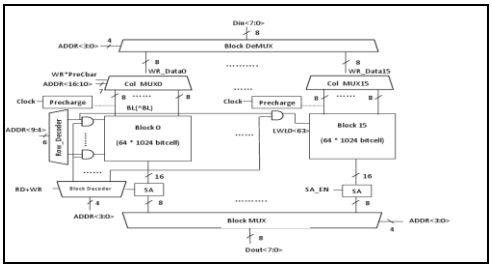


Figure 1. *Block Diagram of the 1MB SRAM unit*

2.2 Bit Cell Design
For this design review, our team opted to showcase the functionality of one 6T bit cell. Multiple bit cells aggregate to create one block. Each block is then assembled to create the full 1MB of memory. By simulating a single bit cell, we hope to prove that our SRAM works at the lowest level. This allows us to be confident that the 1MB cell will behave as expected when we assemble all the blocks.

Our 6T bit cell is designed by cross coupling two inverters. Access to the cross coupled inverters managed two identical NMOS transistors connected to a Word Line (WL). The word line operates only when reading or writing to the bit cell. In the idle stage, the world line is low and the bit cell is stagnant. Similarly, we designed our 6T bit cells with vertical access lines call Bit Line (BL) and Bit Line Bar (BLB) which moderate the actual reads and writes to the cell.

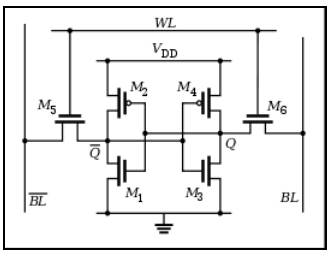


Figure 2: *Standard 6T Bit-Cell Design*

3. SIMULATION RESULTS
The progress made by our team can be seen in the simulation results of our 6T bit cell. Each signal, WL, BL, BLB, read, write, clock, precharge and output, all behave as expected. We would like to make note of the effects of two of our design decisions. To begin, our driver for the precharge signal is not strong enough to force both bit lines to be a full 1 during reads currently. We plan on sizing this to conserve power in the future. The next revision of the design will also likely buffer the read, write and data signals with a register, which will create synchronous inputs to our block. This will allow the cell to hold data without the risk of data corruption or loss. Currently, there are spikes in the simulated results due to overlap of read & write signals in our test bench.

4. NEXT STEPS
The following is a list of completed tasks prior to the formal submission of our design proposal. The documentation of these tasks is appended to the end of this design report.

- ✓ Block Diagram showing arrangement of major SRAM components
- ✓ Gate level netlist of one block of the array
- ✓ Timing diagram for the memory specifically showing the read and write operations
- ✓ A functional bit-cell layout
- ✓ Simulation results

Tasks to be completed following the design proposal:

- Revised memory block design that incorporates registers and appropriate logical effort sizing.
- Assembly of the large 1MB block of memory via netlist
- Comprehensive layout of the 1MB SRAM
- Extensive testing of the SRAM block (includes simulation of key signals and inputs)

5. ACKNOWLEDGMENTS

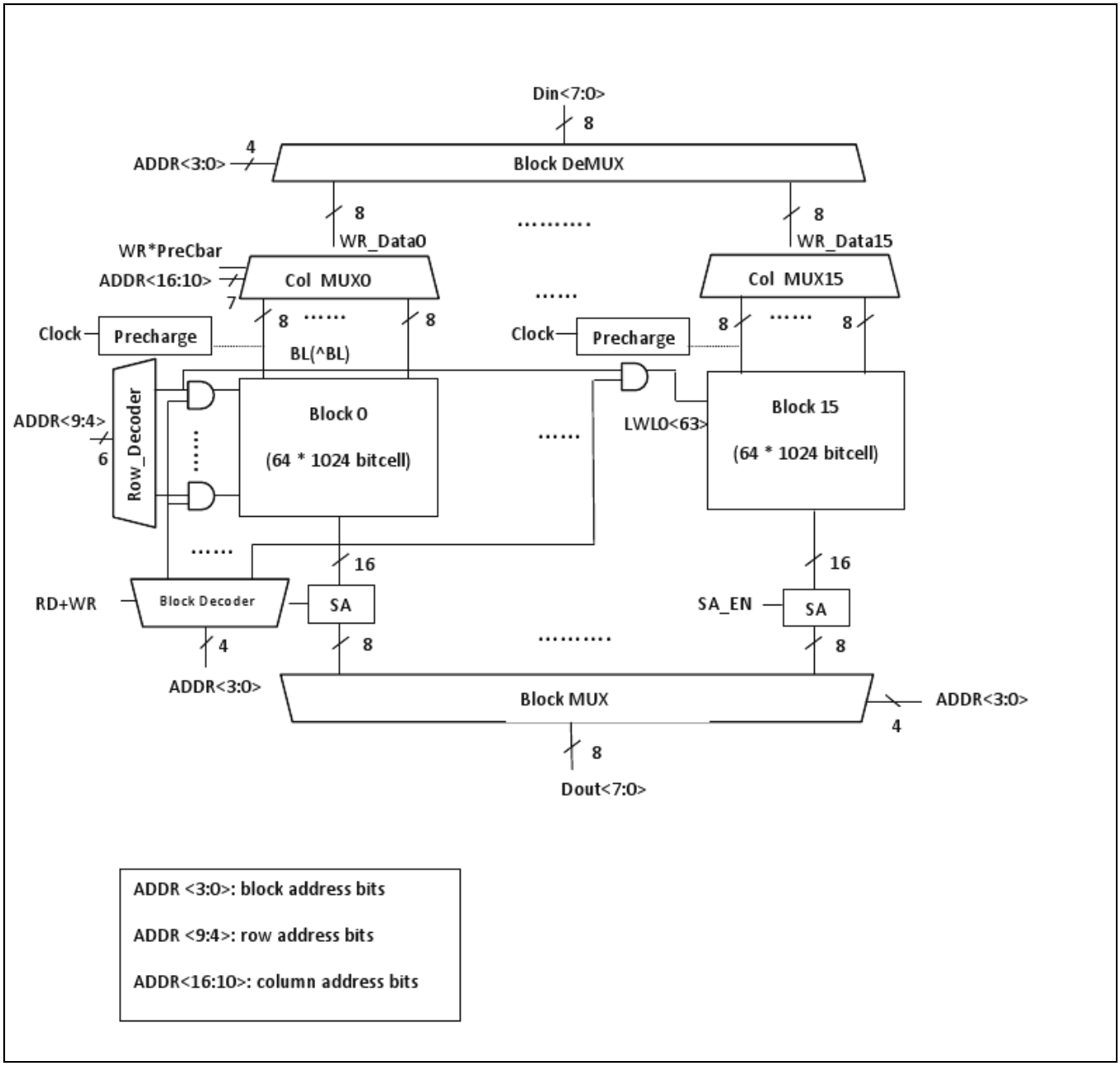
We would like to thank Professor Stan and Mehdi Sadi for their guidance and tutelage on this first design review.

6. REFERENCES

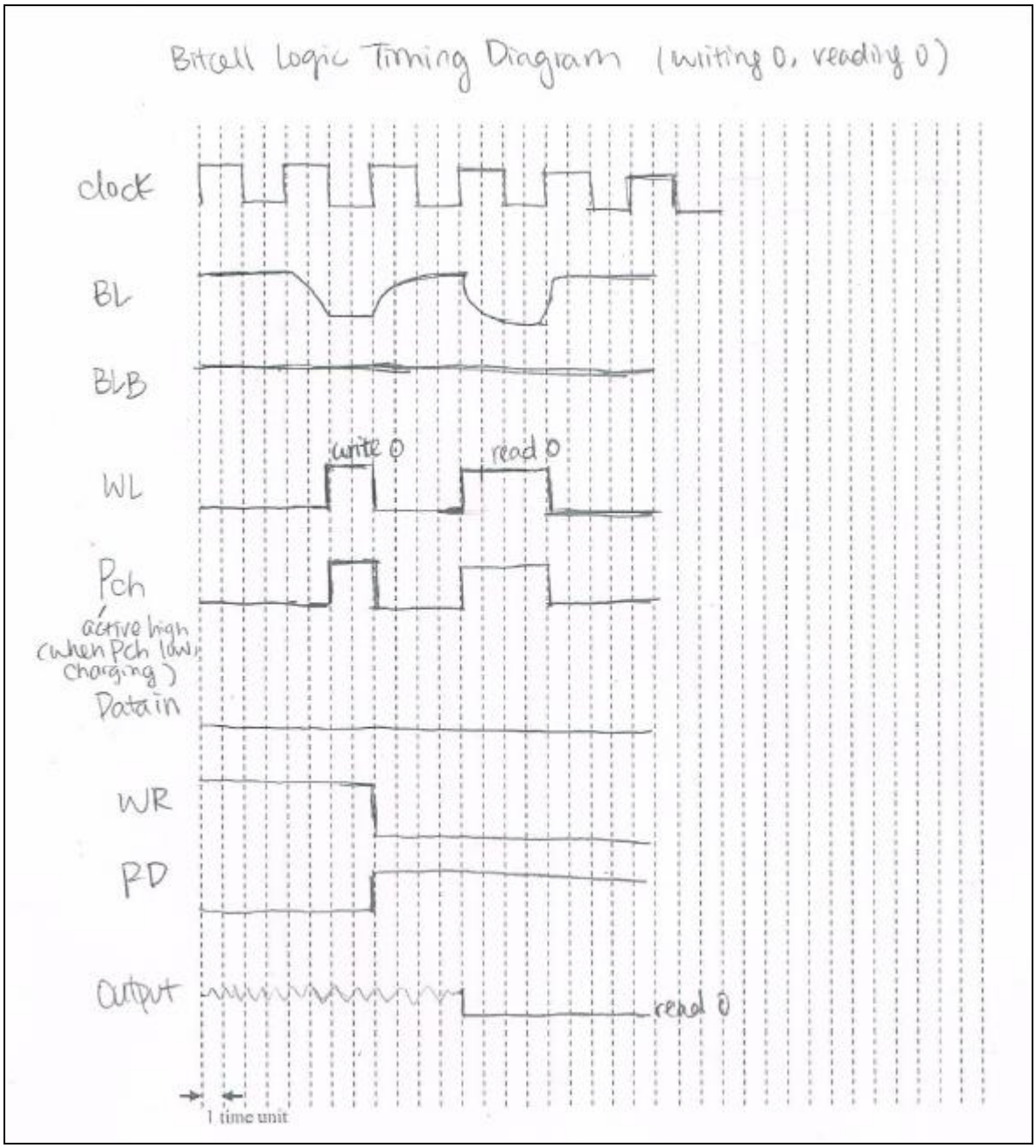
[1] Rabaey, J., Chandrakasan A., Nikolic, B., *Digital Integrated Circuits (2nd Edition)*, (Dec. 24, 2002)

[2] 6T Bit-cell design picture, *http://en.wikipedia.org/wiki/Static_random-access_memory*

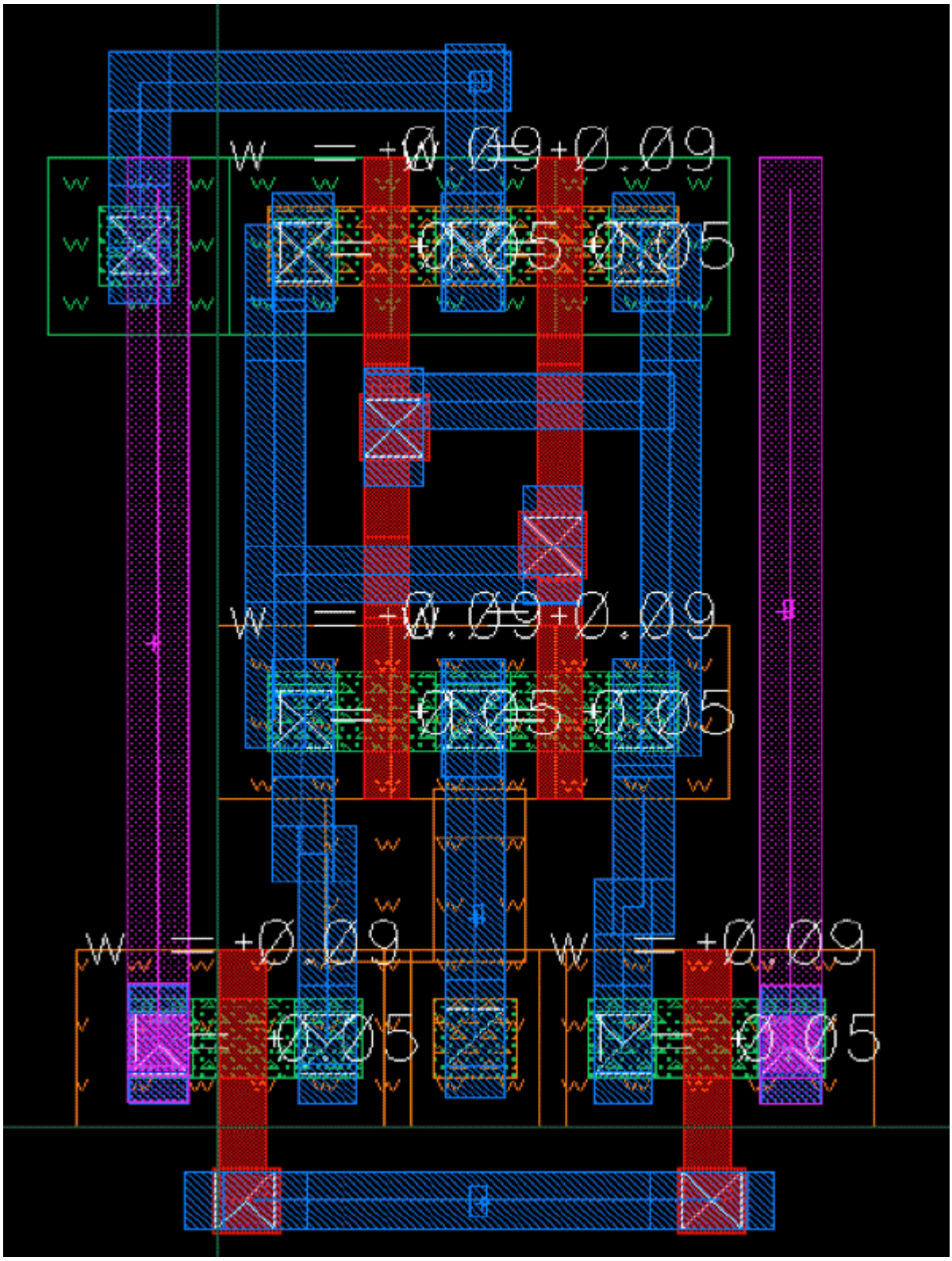
Block Diagram



Timing Diagram

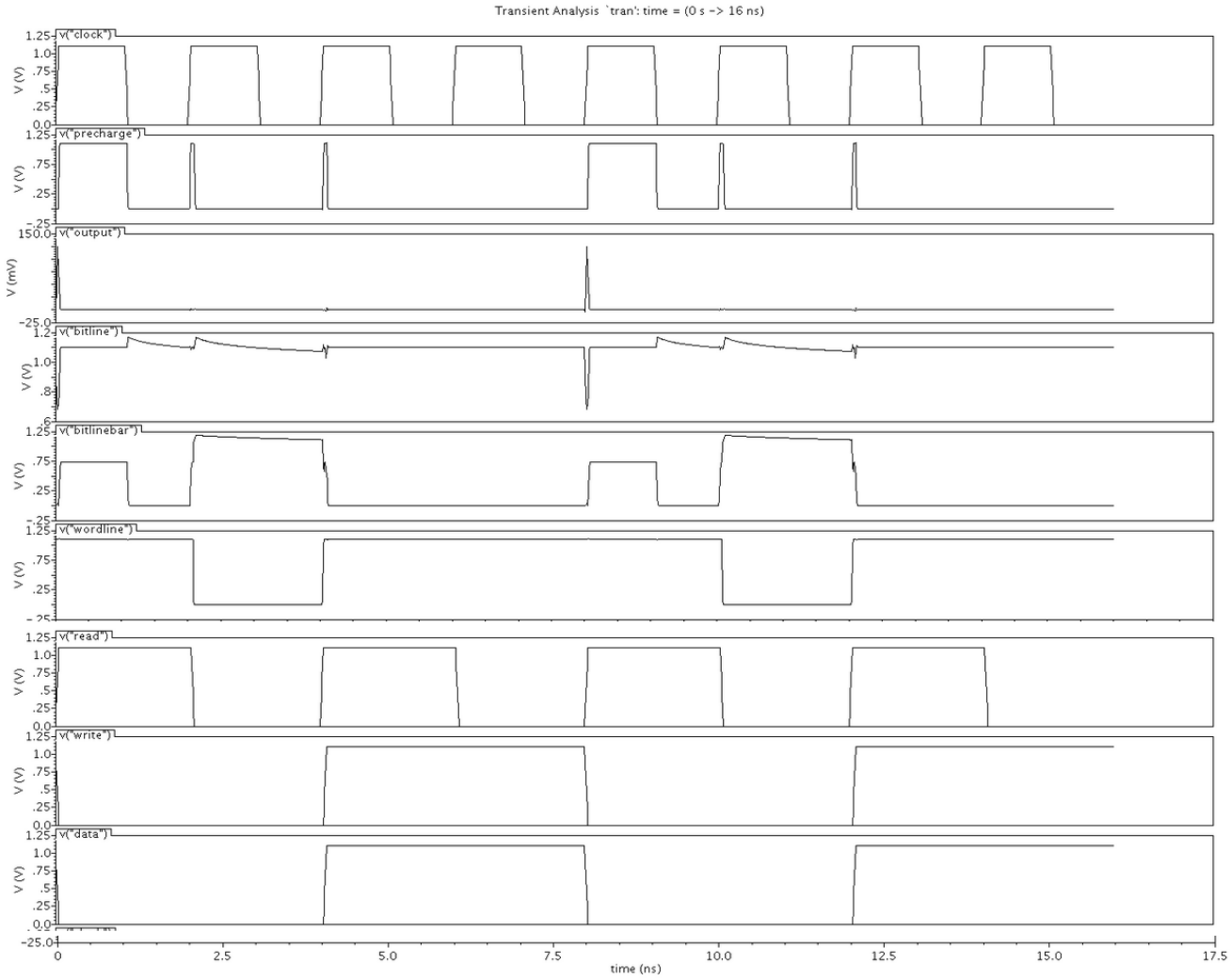


Bitcell layout



Simulation Results

Regular Simulation:



Process Corner Simulation (V=1.2 V, Temp = 0^{o} C):

Cadence Netlist:

```
simulator lang=spectre

include
"/app/lib/freepdk45/trunk/ncsu_basekit/models/hspice/tran_models/models_nom/NMOS_VTL
.inc"
include
"/app/lib/freepdk45/trunk/ncsu_basekit/models/hspice/tran_models/models_nom/PMOS_VTL
.inc"

// Cell name: SenseAmp
// Function: basic differential sense amplifier circuit
// Inputs: bit, bitbar, SE
// Outputs: Out
subckt SenseAmp VDD VSS bit bitbar SE Out
parameters wp=180n wn=90n ln=50n lp=50n
        M1 (net0 bit net1 VSS) NMOS_VTL w=wn l=ln
        M2 (y bitbar net1 VSS) NMOS_VTL w=wn l=ln
        M3 (net0 net0 VDD VDD) PMOS_VTL w=wp l=lp
        M4 (y net0 VDD VDD) PMOS_VTL w=wp l=lp
        M5 (net1 SE VSS VSS) NMOS_VTL w=wn l=ln
        M6 (Out y VSS VSS) NMOS_VTL w=wn l=ln
        M7 (Out y VDD VDD) PMOS_VTL w=wp l=lp
Ends SenseAmp

// 6-input AND
subckt And6 VDD VSS a0 a1 a2 a3 a4 a5 out
parameters wn=540n wp=180n lpn=50n
        M0 (p1 a0 VSS VSS) NMOS_VTL w=wn l=lpn
        M1 (p2 a1 p1 VSS) NMOS_VTL w=wn l=lpn
        M2 (p3 a2 p2 VSS) NMOS_VTL w=wn l=lpn
        M3 (p4 a3 p3 VSS) NMOS_VTL w=wn l=lpn
        M4 (p5 a4 p4 VSS) NMOS_VTL w=wn l=lpn
        M5 (mid a5 p5 VSS) NMOS_VTL w=wn l=lpn
        M6 (mid a0 VDD VDD) PMOS_VTL w=wp l=lpn
        M7 (mid a1 VDD VDD) PMOS_VTL w=wp l=lpn
        M8 (mid a2 VDD VDD) PMOS_VTL w=wp l=lpn
        M9 (mid a3 VDD VDD) PMOS_VTL w=wp l=lpn
        M10 (mid a4 VDD VDD) PMOS_VTL w=wp l=lpn
        M11 (mid a5 VDD VDD) PMOS_VTL w=wp l=lpn
        I0 (VDD VSS mid out) Inverter
ends And6

// 3-input And
subckt And3 VDD VSS a0 a1 a2 out
parameters wn=270n wp=180n lpn=50n
        M0 (p1 a0 VSS VSS) NMOS_VTL w=wn l=lpn
        M1 (p2 a1 p1 VSS) NMOS_VTL w=wn l=lpn
        M2 (mid a2 p2 VSS) NMOS_VTL w=wn l=lpn
        M3 (mid a0 VDD VDD) PMOS_VTL w=wp l=lpn
        M4 (mid a1 VDD VDD) PMOS_VTL w=wp l=lpn
        M5 (mid a2 VDD VDD) PMOS_VTL w=wp l=lpn
        I0 (VDD VSS mid out) Inverter
ends And3

// 2-input AND
subckt And2 VDD VSS a0 a1 out
parameters wn=180n wp=180n lpn=50n
        M0 (p1 a0 VSS VSS) NMOS_VTL w=wn l=lpn
        M1 (mid a1 p1 VSS) NMOS_VTL w=wn l=lpn
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        M2 (mid a0 VDD VDD) PMOS_VTL w=wn l=lpn
        M3 (mid a1 VDD VDD) PMOS_VTL w=wn l=lpn
        I0 (VDD VSS mid out) Inverter
ends And2

// Precharge logic
subckt Precharge VDD VSS clock write precharge
        I0 (VDD VSS write writeb) Inverter
        A0 (VDD VSS clock writeb precharge) And2
ends Precharge

// Column Decoder
subckt ColDecoder VDD VSS a0 a1 a2 a3 a4 C00000 C00001 C00010 C00011 C00100 C00101
C00110 C00111 C01000 C01001 C01010 C01011 C01100 C01101 C01110 C01111 C10000 C10001
C10010 C10011 C10100 C10101 C10110 C10111 C11000 C11001 C11010 C11011 C11100 C11101
C11110 C11111 write
        I0 (VDD VSS a0 a0b) Inverter
        I1 (VDD VSS a1 a1b) Inverter
        I2 (VDD VSS a2 a2b) Inverter
        I3 (VDD VSS a3 a3b) Inverter
        I4 (VDD VSS a4 a4b) Inverter
        N00000 (VDD VSS a0b a1b a2b a3b a4b write C00000) AND6
        N00001 (VDD VSS a0b a1b a2b a3b a4 write C00001) AND6
        N00010 (VDD VSS a0b a1b a2b a3 a4b write C00010) AND6
        N00011 (VDD VSS a0b a1b a2b a3 a4 write C00011) AND6
        N00100 (VDD VSS a0b a1b a2 a3b a4b write C00100) AND6
        N00101 (VDD VSS a0b a1b a2 a3b a4 write C00101) AND6
        N00110 (VDD VSS a0b a1b a2 a3 a4b write C00110) AND6
        N00111 (VDD VSS a0b a1b a2 a3 a4 write C00111) AND6
        N01000 (VDD VSS a0b a1 a2b a3b a4b write C01000) AND6
        N01001 (VDD VSS a0b a1 a2b a3b a4 write C01001) AND6
        N01010 (VDD VSS a0b a1 a2b a3 a4b write C01010) AND6
        N01011 (VDD VSS a0b a1 a2b a3 a4 write C01011) AND6
        N01100 (VDD VSS a0b a1 a2 a3b a4b write C01100) AND6
        N01101 (VDD VSS a0b a1 a2 a3b a4 write C01101) AND6
        N01110 (VDD VSS a0b a1 a2 a3 a4b write C01110) AND6
        N01111 (VDD VSS a0b a1 a2 a3 a4 write C01111) AND6
        N10000 (VDD VSS a0 a1b a2b a3b a4b write C10000) AND6
        N10001 (VDD VSS a0 a1b a2b a3b a4 write C10001) AND6
        N10010 (VDD VSS a0 a1b a2b a3 a4b write C10010) AND6
        N10011 (VDD VSS a0 a1b a2b a3 a4 write C10011) AND6
        N10100 (VDD VSS a0 a1b a2 a3b a4b write C10100) AND6
        N10101 (VDD VSS a0 a1b a2 a3b a4 write C10101) AND6
        N10110 (VDD VSS a0 a1b a2 a3 a4b write C10110) AND6
        N10111 (VDD VSS a0 a1b a2 a3 a4 write C10111) AND6
        N11000 (VDD VSS a0 a1 a2b a3b a4b write C11000) AND6
        N11001 (VDD VSS a0 a1 a2b a3b a4 write C11001) AND6
        N11010 (VDD VSS a0 a1 a2b a3 a4b write C11010) AND6
        N11011 (VDD VSS a0 a1 a2b a3 a4 write C11011) AND6
        N11100 (VDD VSS a0 a1 a2 a3b a4b write C11100) AND6
        N11101 (VDD VSS a0 a1 a2 a3b a4 write C11101) AND6
        N11110 (VDD VSS a0 a1 a2 a3 a4b write C11110) AND6
        N11111 (VDD VSS a0 a1 a2 a3 a4 write C11111) AND6
ends ColDecoder

// Row Decoder
subckt RowDecoder VDD VSS a0 a1 a2 a3 a4 a5 WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9
WL10 WL11 WL12 WL13 WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26
WL27 WL28 WL29 WL30 WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43
WL44 WL45 WL46 WL47 WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60
WL61 WL62 WL63
        I0 (VDD VSS a0 a0b) Inverter
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I1 (VDD VSS a1 a1b) Inverter
I2 (VDD VSS a2 a2b) Inverter
I3 (VDD VSS a3 a3b) Inverter
I4 (VDD VSS a4 a4b) Inverter
I5 (VDD VSS a5 a5b) Inverter
N000000 (VDD VSS a0b a1b a2b a3b a4b a5b WL0) AND6
N000001 (VDD VSS a0b a1b a2b a3b a4b a5 WL1) AND6
N000010 (VDD VSS a0b a1b a2b a3b a4 a5b WL2) AND6
N000011 (VDD VSS a0b a1b a2b a3b a4 a5 WL3) AND6
N000100 (VDD VSS a0b a1b a2b a3 a4b a5b WL4) AND6
N000101 (VDD VSS a0b a1b a2b a3 a4b a5 WL5) AND6
N000110 (VDD VSS a0b a1b a2b a3 a4 a5b WL6) AND6
N000111 (VDD VSS a0b a1b a2b a3 a4 a5 WL7) AND6
N001000 (VDD VSS a0b a1b a2 a3b a4b a5b WL8) AND6
N001001 (VDD VSS a0b a1b a2 a3b a4b a5 WL9) AND6
N001010 (VDD VSS a0b a1b a2 a3b a4 a5b WL10) AND6
N001011 (VDD VSS a0b a1b a2 a3b a4 a5 WL11) AND6
N001100 (VDD VSS a0b a1b a2 a3 a4b a5b WL12) AND6
N001101 (VDD VSS a0b a1b a2 a3 a4b a5 WL13) AND6
N001110 (VDD VSS a0b a1b a2 a3 a4 a5b WL14) AND6
N001111 (VDD VSS a0b a1b a2 a3 a4 a5 WL15) AND6
N010000 (VDD VSS a0b a1 a2b a3b a4b a5b WL16) AND6
N010001 (VDD VSS a0b a1 a2b a3b a4b a5 WL17) AND6
N010010 (VDD VSS a0b a1 a2b a3b a4 a5b WL18) AND6
N010011 (VDD VSS a0b a1 a2b a3b a4 a5 WL19) AND6
N010100 (VDD VSS a0b a1 a2b a3 a4b a5b WL20) AND6
N010101 (VDD VSS a0b a1 a2b a3 a4b a5 WL21) AND6
N010110 (VDD VSS a0b a1 a2b a3 a4 a5b WL22) AND6
N010111 (VDD VSS a0b a1 a2b a3 a4 a5 WL23) AND6
N011000 (VDD VSS a0b a1 a2 a3b a4b a5b WL24) AND6
N011001 (VDD VSS a0b a1 a2 a3b a4b a5 WL25) AND6
N011010 (VDD VSS a0b a1 a2 a3b a4 a5b WL26) AND6
N011011 (VDD VSS a0b a1 a2 a3b a4 a5 WL27) AND6
N011100 (VDD VSS a0b a1 a2 a3 a4b a5b WL28) AND6
N011101 (VDD VSS a0b a1 a2 a3 a4b a5 WL29) AND6
N011110 (VDD VSS a0b a1 a2 a3 a4 a5b WL30) AND6
N011111 (VDD VSS a0b a1 a2 a3 a4 a5 WL31) AND6
N100000 (VDD VSS a0 a1b a2b a3b a4b a5b WL32) AND6
N100001 (VDD VSS a0 a1b a2b a3b a4b a5 WL33) AND6
N100010 (VDD VSS a0 a1b a2b a3b a4 a5b WL34) AND6
N100011 (VDD VSS a0 a1b a2b a3b a4 a5 WL35) AND6
N100100 (VDD VSS a0 a1b a2b a3 a4b a5b WL36) AND6
N100101 (VDD VSS a0 a1b a2b a3 a4b a5 WL37) AND6
N100110 (VDD VSS a0 a1b a2b a3 a4 a5b WL38) AND6
N100111 (VDD VSS a0 a1b a2b a3 a4 a5 WL39) AND6
N101000 (VDD VSS a0 a1b a2 a3b a4b a5b WL40) AND6
N101001 (VDD VSS a0 a1b a2 a3b a4b a5 WL41) AND6
N101010 (VDD VSS a0 a1b a2 a3b a4 a5b WL42) AND6
N101011 (VDD VSS a0 a1b a2 a3b a4 a5 WL43) AND6
N101100 (VDD VSS a0 a1b a2 a3 a4b a5b WL44) AND6
N101101 (VDD VSS a0 a1b a2 a3 a4b a5 WL45) AND6
N101110 (VDD VSS a0 a1b a2 a3 a4 a5b WL46) AND6
N101111 (VDD VSS a0 a1b a2 a3 a4 a5 WL47) AND6
N110000 (VDD VSS a0 a1 a2b a3b a4b a5b WL48) AND6
N110001 (VDD VSS a0 a1 a2b a3b a4b a5 WL49) AND6
N110010 (VDD VSS a0 a1 a2b a3b a4 a5b WL50) AND6
N110011 (VDD VSS a0 a1 a2b a3b a4 a5 WL51) AND6
N110100 (VDD VSS a0 a1 a2b a3 a4b a5b WL52) AND6
N110101 (VDD VSS a0 a1 a2b a3 a4b a5 WL53) AND6
N110110 (VDD VSS a0 a1 a2b a3 a4 a5b WL54) AND6
N110111 (VDD VSS a0 a1 a2b a3 a4 a5 WL55) AND6
N111000 (VDD VSS a0 a1 a2 a3b a4b a5b WL56) AND6
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        N111001 (VDD VSS a0 a1 a2 a3b a4b a5 WL57) AND6
        N111010 (VDD VSS a0 a1 a2 a3b a4 a5b WL58) AND6
        N111011 (VDD VSS a0 a1 a2 a3b a4 a5 WL59) AND6
        N111100 (VDD VSS a0 a1 a2 a3 a4b a5b WL60) AND6
        N111101 (VDD VSS a0 a1 a2 a3 a4b a5 WL61) AND6
        N111110 (VDD VSS a0 a1 a2 a3 a4 a5b WL62) AND6
        N111111 (VDD VSS a0 a1 a2 a3 a4 a5 WL63) AND6
ends RowDecoder

// 2:1 Mux
// Standard width: 4*90n = 360nm
subckt Mux2 VDD VSS in1 in2 s sb out
parameters wn=90n wp=90n
        // T-gate
    M0 (out sb in1 VSS) NMOS_VTL w=wn l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n
    M1 (out s in1 VDD) PMOS_VTL w=wp l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n
pd=390.0n
    // T-gate
    M2 (out s in2 VSS) NMOS_VTL w=wn l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n
    M3 (out sb in2 VDD) PMOS_VTL w=wp l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n
pd=390.0n
ends Mux2

// 4:1 Mux
// Total width: 4*Mux2 = 1210nm
subckt Mux4 VDD VSS in0 in1 in2 in3 s0 s1 out
parameters wpp=90n wnn=90n
        I0 (VDD VSS s0 s0b) Inverter
        I1 (VDD VSS s1 s1b) Inverter
        M0 (VDD VSS in0 in1 s0 s0b 0or1) Mux2 wp=wpp wn=wnn
        M1 (VDD VSS in2 in3 s0 s0b 2or3) Mux2 wp=wpp wn=wnn
        M4 (VDD VSS 0or1 2or3 s1 s1b out) Mux2 wp=wpp wn=wnn
ends Mux4

subckt Mux32 VDD VSS in00000 in00001 in00010 in00011 in00100 in00101 in00110 in00111
in01000 in01001 in01010 in01011 in01100 in01101 in01110 in01111 in10000 in10001
in10010 in10011 in10100 in10101 in10110 in10111 in11000 in11001 in11010 in11011
in11100 in11101 in11110 in11111 sel0 sel1 sel2 sel3 sel4 out
        M0 (VDD VSS in00000 in00001 in00010 in00011 sel3 sel4 0to3) Mux4
        M1 (VDD VSS in00100 in00101 in00110 in00111 sel3 sel4 4to7) Mux4
        M2 (VDD VSS in01000 in01001 in01010 in01011 sel3 sel4 8to11) Mux4
        M3 (VDD VSS in01100 in01101 in01110 in01111 sel3 sel4 12to15) Mux4
        M4 (VDD VSS in10000 in10001 in10010 in10011 sel3 sel4 16to19) Mux4
        M5 (VDD VSS in10100 in10101 in10110 in10111 sel3 sel4 20to23) Mux4
        M6 (VDD VSS in11000 in11001 in11010 in11011 sel3 sel4 24to27) Mux4
        M7 (VDD VSS in11100 in11101 in11110 in11111 sel3 sel4 28to31) Mux4
        M8 (VDD VSS 0to3 4to7 8to11 12to15 sel1 sel2 top) Mux4
        M9 (VDD VSS 16to19 20to23 24to27 28to31 sel1 sel2 bot) Mux4
        I0 (VDD VSS sel0 sel0b) Inverter
        M10 (VDD VSS top bot sel0 sel0b out) Mux2
ends Mux32

subckt BitCell VDD VSS WL BL BLB
parameters wp24=90n wn13=160n wn56=108n lpn=50n
        M1 (Q QB VSS VSS) NMOS_VTL w=wn13 l=lpn
        M2 (Q QB VDD VDD) NMOS_VTL w=wn24 l=lpn
        M3 (QB Q VSS VSS) NMOS_VTL w=wn13 l=lpn
        M4 (QB Q VDD VDD) PMOS_VTL w=wn24 l=lpn
        M5 (Q WL BL VSS) NMOS_VTL w=wn56 l=lpn
        M6 (QB WL BLB VSS) NMOS_VTL w=wn56 l=lpn
ends BitCell
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```
subckt enabledBuffer VDD VSS in out en
parameters wp=180n wn=90n lpn=50n
        M0 (mid in VSS VSS) NMOS_VTL w=wn l=lpn
        M1 (mid in VDD VDD) PMOS_VTL w=wp l=lpn
        M2 (botint mid VSS VSS) NMOS_VTL w=wn l=lpn
        M3 (topint mid VDD VDD) PMOS_VTL w=wp l=lpn
        M4 (out en botint VSS) NMOS_VTL w=wn l=lpn
        M5 (out en topint VDD) PMOS_VTL w=wp l=lpn
ends enabledBuffer

subckt Inverter VDD VSS in out
parameters wp=180n wn=90n lpn=50n
        M0 (out in VDD VDD) PMOS_VTL
        M1 (out in VSS VSS) NMOS_VTL
ends Inverter

subckt Word8 VDD VSS WL BL0 BLB0 BL1 BLB1 BL2 BLB2 BL3 BLB3 BL4 BLB4 BL5 BLB5 BL6
BLB6 BL7 BLB7
        B0 (VDD VSS WL BL0 BLB0) BitCell
        B1 (VDD VSS WL BL1 BLB1) BitCell
        B2 (VDD VSS WL BL2 BLB2) BitCell
        B3 (VDD VSS WL BL3 BLB3) BitCell
        B4 (VDD VSS WL BL4 BLB4) BitCell
        B5 (VDD VSS WL BL5 BLB5) BitCell
        B6 (VDD VSS WL BL6 BLB6) BitCell
        B7 (VDD VSS WL BL7 BLB7) BitCell
ends Word8

subckt Row VDD VSS WL SEL0 SEL1 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04
BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13
BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23
BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32
BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37
        W0 (VDD VSS WL BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07) Word8
        W1 (VDD VSS WL BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15
BLB15 BL16 BLB16 BL17 BLB17) Word8
        W2 (VDD VSS WL BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25
BLB25 BL26 BLB26 BL27 BLB27) Word8
        W3 (VDD VSS WL BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35
BLB35 BL36 BLB36 BL37 BLB37) Word8
ends Row

// Remember write is going to be dependent on the writing line, so you need to
change write to be write versus the word.
// Write into each column will be a column decoder anded with the global write
value.
subckt Column VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q0 q1 q2 q3 q4 q5 q6 q7 sel0 sel1 write read
        // get opposites in case we're writing
        I0 (VDD VSS d0 db0) Inverter
        I1 (VDD VSS d1 db1) Inverter
        I2 (VDD VSS d2 db2) Inverter
        I3 (VDD VSS d3 db3) Inverter
        I4 (VDD VSS d4 db4) Inverter
        I5 (VDD VSS d5 db5) Inverter
        I6 (VDD VSS d6 db6) Inverter
        I7 (VDD VSS d7 db7) Inverter
```

```
I8 (VDD VSS sel0 sel0b) Inverter
I9 (VDD VSS sel1 sel1b) Inverter
I10 (VDD VSS clock clockb) Inverter

// Determine which write lines to assert if we're actually writing
A0 (VDD VSS sel0b sel1b write write0) And3
A1 (VDD VSS sel0b sel1 write write1) And3
A2 (VDD VSS sel0 sel1b write write2) And3
A3 (VDD VSS sel0 sel1 write write3) And3

// Figure out the precharge lines
P0 (VDD VSS clock write0 precharge0) Precharge
P1 (VDD VSS clock write1 precharge1) Precharge
P2 (VDD VSS clock write2 precharge2) Precharge
P3 (VDD VSS clock write3 precharge3) Precharge

// Get local read lines to save power for sense amps
A4 (VDD VSS sel0b sel1b read read0) And3
A5 (VDD VSS sel0b sel1 read read1) And3
A6 (VDD VSS sel0 sel1b read read2) And3
A7 (VDD VSS sel0 sel1 read read3) And3

// Sense amp enables
S0 (VDD VSS clockb read0 SE0) And2
S1 (VDD VSS clockb read1 SE1) And2
S2 (VDD VSS clockb read2 SE2) And2
S3 (VDD VSS clockb read3 SE3) And3

// precharge buffers in case we're reading
W00 (VDD VSS VDD BL00 precharge0) enabledBuffer
W10 (VDD VSS VDD BL10 precharge1) enabledBuffer
W20 (VDD VSS VDD BL20 precharge2) enabledBuffer
W30 (VDD VSS VDD BL30 precharge3) enabledBuffer
W01 (VDD VSS VDD BL01 precharge0) enabledBuffer
W11 (VDD VSS VDD BL11 precharge1) enabledBuffer
W21 (VDD VSS VDD BL21 precharge2) enabledBuffer
W31 (VDD VSS VDD BL31 precharge3) enabledBuffer
W02 (VDD VSS VDD BL02 precharge0) enabledBuffer
W12 (VDD VSS VDD BL12 precharge1) enabledBuffer
W22 (VDD VSS VDD BL22 precharge2) enabledBuffer
W32 (VDD VSS VDD BL32 precharge3) enabledBuffer
W03 (VDD VSS VDD BL03 precharge0) enabledBuffer
W13 (VDD VSS VDD BL13 precharge1) enabledBuffer
W23 (VDD VSS VDD BL23 precharge2) enabledBuffer
W33 (VDD VSS VDD BL33 precharge3) enabledBuffer
W04 (VDD VSS VDD BL04 precharge0) enabledBuffer
W14 (VDD VSS VDD BL14 precharge1) enabledBuffer
W24 (VDD VSS VDD BL24 precharge2) enabledBuffer
W34 (VDD VSS VDD BL34 precharge3) enabledBuffer
W05 (VDD VSS VDD BL05 precharge0) enabledBuffer
W15 (VDD VSS VDD BL15 precharge1) enabledBuffer
W25 (VDD VSS VDD BL25 precharge2) enabledBuffer
W35 (VDD VSS VDD BL35 precharge3) enabledBuffer
W06 (VDD VSS VDD BL06 precharge0) enabledBuffer
W16 (VDD VSS VDD BL16 precharge1) enabledBuffer
W26 (VDD VSS VDD BL26 precharge2) enabledBuffer
W36 (VDD VSS VDD BL36 precharge3) enabledBuffer
W07 (VDD VSS VDD BL07 precharge0) enabledBuffer
W17 (VDD VSS VDD BL17 precharge1) enabledBuffer
W27 (VDD VSS VDD BL27 precharge2) enabledBuffer
W37 (VDD VSS VDD BL37 precharge3) enabledBuffer
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// precharge buffers in case we're reading
W100 (VDD VSS VDD BLB00 precharge0) enabledBuffer
W110 (VDD VSS VDD BLB10 precharge1) enabledBuffer
W120 (VDD VSS VDD BLB20 precharge2) enabledBuffer
W130 (VDD VSS VDD BLB30 precharge3) enabledBuffer
W101 (VDD VSS VDD BLB01 precharge0) enabledBuffer
W111 (VDD VSS VDD BLB11 precharge1) enabledBuffer
W121 (VDD VSS VDD BLB21 precharge2) enabledBuffer
W131 (VDD VSS VDD BLB31 precharge3) enabledBuffer
W102 (VDD VSS VDD BLB02 precharge0) enabledBuffer
W112 (VDD VSS VDD BLB12 precharge1) enabledBuffer
W122 (VDD VSS VDD BLB22 precharge2) enabledBuffer
W132 (VDD VSS VDD BLB32 precharge3) enabledBuffer
W103 (VDD VSS VDD BLB03 precharge0) enabledBuffer
W113 (VDD VSS VDD BLB13 precharge1) enabledBuffer
W123 (VDD VSS VDD BLB23 precharge2) enabledBuffer
W133 (VDD VSS VDD BLB33 precharge3) enabledBuffer
W104 (VDD VSS VDD BLB04 precharge0) enabledBuffer
W114 (VDD VSS VDD BLB14 precharge1) enabledBuffer
W124 (VDD VSS VDD BLB24 precharge2) enabledBuffer
W134 (VDD VSS VDD BLB34 precharge3) enabledBuffer
W105 (VDD VSS VDD BLB05 precharge0) enabledBuffer
W115 (VDD VSS VDD BLB15 precharge1) enabledBuffer
W125 (VDD VSS VDD BLB25 precharge2) enabledBuffer
W135 (VDD VSS VDD BLB35 precharge3) enabledBuffer
W106 (VDD VSS VDD BLB06 precharge0) enabledBuffer
W116 (VDD VSS VDD BLB16 precharge1) enabledBuffer
W126 (VDD VSS VDD BLB26 precharge2) enabledBuffer
W136 (VDD VSS VDD BLB36 precharge3) enabledBuffer
W107 (VDD VSS VDD BLB07 precharge0) enabledBuffer
W117 (VDD VSS VDD BLB17 precharge1) enabledBuffer
W127 (VDD VSS VDD BLB27 precharge2) enabledBuffer
W137 (VDD VSS VDD BLB37 precharge3) enabledBuffer

// write buffers in case we're writing
W00 (VDD VSS d0 BL00 write0) enabledBuffer
W10 (VDD VSS d0 BL10 write1) enabledBuffer
W20 (VDD VSS d0 BL20 write2) enabledBuffer
W30 (VDD VSS d0 BL30 write3) enabledBuffer
W01 (VDD VSS d1 BL01 write0) enabledBuffer
W11 (VDD VSS d1 BL11 write1) enabledBuffer
W21 (VDD VSS d1 BL21 write2) enabledBuffer
W31 (VDD VSS d1 BL31 write3) enabledBuffer
W02 (VDD VSS d2 BL02 write0) enabledBuffer
W12 (VDD VSS d2 BL12 write1) enabledBuffer
W22 (VDD VSS d2 BL22 write2) enabledBuffer
W32 (VDD VSS d2 BL32 write3) enabledBuffer
W03 (VDD VSS d3 BL03 write0) enabledBuffer
W13 (VDD VSS d3 BL13 write1) enabledBuffer
W23 (VDD VSS d3 BL23 write2) enabledBuffer
W33 (VDD VSS d3 BL33 write3) enabledBuffer
W04 (VDD VSS d4 BL04 write0) enabledBuffer
W14 (VDD VSS d4 BL14 write1) enabledBuffer
W24 (VDD VSS d4 BL24 write2) enabledBuffer
W34 (VDD VSS d4 BL34 write3) enabledBuffer
W05 (VDD VSS d5 BL05 write0) enabledBuffer
W15 (VDD VSS d5 BL15 write1) enabledBuffer
W25 (VDD VSS d5 BL25 write2) enabledBuffer
W35 (VDD VSS d5 BL35 write3) enabledBuffer
W06 (VDD VSS d6 BL06 write0) enabledBuffer
W16 (VDD VSS d6 BL16 write1) enabledBuffer
W26 (VDD VSS d6 BL26 write2) enabledBuffer
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W36 (VDD VSS d6 BL36 write3) enabledBuffer
W07 (VDD VSS d7 BL07 write0) enabledBuffer
W17 (VDD VSS d7 BL17 write1) enabledBuffer
W27 (VDD VSS d7 BL27 write2) enabledBuffer
W37 (VDD VSS d7 BL37 write3) enabledBuffer

// write buffers in case we're writing
W100 (VDD VSS db0 BLB00 write0) enabledBuffer
W110 (VDD VSS db0 BLB10 write1) enabledBuffer
W120 (VDD VSS db0 BLB20 write2) enabledBuffer
W130 (VDD VSS db0 BLB30 write3) enabledBuffer
W101 (VDD VSS db1 BLB01 write0) enabledBuffer
W111 (VDD VSS db1 BLB11 write1) enabledBuffer
W121 (VDD VSS db1 BLB21 write2) enabledBuffer
W131 (VDD VSS db1 BLB31 write3) enabledBuffer
W102 (VDD VSS db2 BLB02 write0) enabledBuffer
W112 (VDD VSS db2 BLB12 write1) enabledBuffer
W122 (VDD VSS db2 BLB22 write2) enabledBuffer
W132 (VDD VSS db2 BLB32 write3) enabledBuffer
W103 (VDD VSS db3 BLB03 write0) enabledBuffer
W113 (VDD VSS db3 BLB13 write1) enabledBuffer
W123 (VDD VSS db3 BLB23 write2) enabledBuffer
W133 (VDD VSS db3 BLB33 write3) enabledBuffer
W104 (VDD VSS db4 BLB04 write0) enabledBuffer
W114 (VDD VSS db4 BLB14 write1) enabledBuffer
W124 (VDD VSS db4 BLB24 write2) enabledBuffer
W134 (VDD VSS db4 BLB34 write3) enabledBuffer
W105 (VDD VSS db5 BLB05 write0) enabledBuffer
W115 (VDD VSS db5 BLB15 write1) enabledBuffer
W125 (VDD VSS db5 BLB25 write2) enabledBuffer
W135 (VDD VSS db5 BLB35 write3) enabledBuffer
W106 (VDD VSS db6 BLB06 write0) enabledBuffer
W116 (VDD VSS db6 BLB16 write1) enabledBuffer
W126 (VDD VSS db6 BLB26 write2) enabledBuffer
W136 (VDD VSS db6 BLB36 write3) enabledBuffer
W107 (VDD VSS db7 BLB07 write0) enabledBuffer
W117 (VDD VSS db7 BLB17 write1) enabledBuffer
W127 (VDD VSS db7 BLB27 write2) enabledBuffer
W137 (VDD VSS db7 BLB37 write3) enabledBuffer

// Sense amps at the bottom of each bit line
S00 (VDD VSS BL00 BLB00 out00 SE0) SenseAmp
S10 (VDD VSS BL10 BLB10 out10 SE1) SenseAmp
S20 (VDD VSS BL20 BLB20 out20 SE2) SenseAmp
S30 (VDD VSS BL30 BLB30 out30 SE3) SenseAmp
S01 (VDD VSS BL01 BLB01 out01 SE0) SenseAmp
S11 (VDD VSS BL11 BLB11 out11 SE1) SenseAmp
S21 (VDD VSS BL21 BLB21 out21 SE2) SenseAmp
S31 (VDD VSS BL31 BLB31 out31 SE3) SenseAmp
S02 (VDD VSS BL02 BLB02 out02 SE0) SenseAmp
S12 (VDD VSS BL12 BLB12 out12 SE1) SenseAmp
S22 (VDD VSS BL22 BLB22 out22 SE2) SenseAmp
S32 (VDD VSS BL32 BLB32 out32 SE3) SenseAmp
S03 (VDD VSS BL03 BLB03 out03 SE0) SenseAmp
S13 (VDD VSS BL13 BLB13 out13 SE1) SenseAmp
S23 (VDD VSS BL23 BLB23 out23 SE2) SenseAmp
S33 (VDD VSS BL33 BLB33 out33 SE3) SenseAmp
S04 (VDD VSS BL04 BLB04 out04 SE0) SenseAmp
S14 (VDD VSS BL14 BLB14 out14 SE1) SenseAmp
S24 (VDD VSS BL24 BLB24 out24 SE2) SenseAmp
S34 (VDD VSS BL34 BLB34 out34 SE3) SenseAmp
S05 (VDD VSS BL05 BLB05 out05 SE0) SenseAmp
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        S15 (VDD VSS BL15 BLB15 out15 SE1) SenseAmp
        S25 (VDD VSS BL25 BLB25 out25 SE2) SenseAmp
        S35 (VDD VSS BL35 BLB35 out35 SE3) SenseAmp
        S06 (VDD VSS BL06 BLB06 out06 SE0) SenseAmp
        S16 (VDD VSS BL16 BLB16 out16 SE1) SenseAmp
        S26 (VDD VSS BL26 BLB26 out26 SE2) SenseAmp
        S36 (VDD VSS BL36 BLB36 out36 SE3) SenseAmp
        S07 (VDD VSS BL07 BLB07 out07 SE0) SenseAmp
        S17 (VDD VSS BL17 BLB17 out17 SE1) SenseAmp
        S27 (VDD VSS BL27 BLB27 out27 SE2) SenseAmp
        S37 (VDD VSS BL37 BLB37 out37 SE3) SenseAmp

        // Muxes to choose the output based on input address
        M0 (VDD VSS out00 out01 out02 out03 q0) Mux4
        M1 (VDD VSS out10 out11 out12 out13 q1) Mux4
        M2 (VDD VSS out20 out21 out22 out23 q2) Mux4
        M3 (VDD VSS out30 out31 out32 out33 q3) Mux4
        M4 (VDD VSS out40 out41 out42 out43 q4) Mux4
        M5 (VDD VSS out50 out51 out52 out53 q5) Mux4
        M6 (VDD VSS out60 out61 out62 out63 q6) Mux4
        M7 (VDD VSS out70 out71 out72 out73 q7) Mux4

        // Rows
        R0 (VDD VSS WL0 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R1 (VDD VSS WL1 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R2 (VDD VSS WL2 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R3 (VDD VSS WL3 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R4 (VDD VSS WL4 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R5 (VDD VSS WL5 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R6 (VDD VSS WL6 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R7 (VDD VSS WL7 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
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BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R8 (VDD VSS WL8 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R9 (VDD VSS WL9 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05
BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14
BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24
BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33
BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R10 (VDD VSS WL10 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R11 (VDD VSS WL11 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R12 (VDD VSS WL12 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R13 (VDD VSS WL13 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R14 (VDD VSS WL14 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R15 (VDD VSS WL15 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R16 (VDD VSS WL16 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R17 (VDD VSS WL17 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R18 (VDD VSS WL18 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R19 (VDD VSS WL19 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R20 (VDD VSS WL20 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R21 (VDD VSS WL21 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R22 (VDD VSS WL22 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R23 (VDD VSS WL23 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R24 (VDD VSS WL24 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R25 (VDD VSS WL25 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R26 (VDD VSS WL26 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R27 (VDD VSS WL27 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R28 (VDD VSS WL28 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R29 (VDD VSS WL29 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R30 (VDD VSS WL30 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R31 (VDD VSS WL31 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14 BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23 BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33 BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

R32 (VDD VSS WL32 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04 BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14

BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R33 (VDD VSS WL33 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R34 (VDD VSS WL34 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R35 (VDD VSS WL35 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R36 (VDD VSS WL36 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R37 (VDD VSS WL37 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R38 (VDD VSS WL38 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R39 (VDD VSS WL39 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R40 (VDD VSS WL40 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R41 (VDD VSS WL41 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R42 (VDD VSS WL42 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R43 (VDD VSS WL43 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R44 (VDD VSS WL44 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23

BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R45 (VDD VSS WL45 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R46 (VDD VSS WL46 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R47 (VDD VSS WL47 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R48 (VDD VSS WL48 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R49 (VDD VSS WL49 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R50 (VDD VSS WL50 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R51 (VDD VSS WL51 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R52 (VDD VSS WL52 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R53 (VDD VSS WL53 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R54 (VDD VSS WL54 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R55 (VDD VSS WL55 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
R56 (VDD VSS WL56 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row

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        R57 (VDD VSS WL57 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R58 (VDD VSS WL58 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R59 (VDD VSS WL59 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R60 (VDD VSS WL60 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R61 (VDD VSS WL61 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R62 (VDD VSS WL62 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
        R63 (VDD VSS WL63 BL00 BLB00 BL01 BLB01 BL02 BLB02 BL03 BLB03 BL04 BLB04
BL05 BLB05 BL06 BLB06 BL07 BLB07 BL10 BLB10 BL11 BLB11 BL12 BLB12 BL13 BLB13 BL14
BLB14 BL15 BLB15 BL16 BLB16 BL17 BLB17 BL20 BLB20 BL21 BLB21 BL22 BLB22 BL23 BLB23
BL24 BLB24 BL25 BLB25 BL26 BLB26 BL27 BLB27 BL30 BLB30 BL31 BLB31 BL32 BLB32 BL33
BLB33 BL34 BLB34 BL35 BLB35 BL36 BLB36 BL37 BLB37) Row
ends Column

subckt Block VDD VSS clock a0 a1 a2 a3 a4 a5 a6 a7 a8 a9 a10 a11 a12 d0 d1 d2 d3 d4
d5 d6 d7 q0 q1 q2 q3 q4 q5 q6 q7 read write
        // Row decoder
        R0 (VDD VSS a0 a1 a2 a3 a4 a5 WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10
WL11 WL12 WL13 WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27
WL28 WL29 WL30 WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44
WL45 WL46 WL47 WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61
WL62 WL63) RowDecoder

        // Column decoder needed
        D0 (VDD VSS a0 a1 a2 a3 a4 write00000 write00001 write00010 write00011
write00100 write00101 write00110 write00111 write01000 write01001 write01010
write01011 write01100 write01101 write01110 write01111 write10000 write10001
write10010 write10011 write10100 write10101 write10110 write10111 write11000
write11001 write11010 write11011 write11100 write11101 write11110 write11111 write )
ColDecoder

        // Columns
        C00000 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q000001 q000002 q000003 q000004 q000005 q000006 q000007 q000008
a11 a12 write00000 read ) Column
```

C00001 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q000011 q000012 q000013 q000014 q000015 q000016 q000017 q000018
a11 a12 write00001 read) Column
C00010 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q000101 q000102 q000103 q000104 q000105 q000106 q000107 q000108
a11 a12 write00010 read) Column
C00011 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q000111 q000112 q000113 q000114 q000115 q000116 q000117 q000118
a11 a12 write00011 read) Column
C00100 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q001001 q001002 q001003 q001004 q001005 q001006 q001007 q001008
a11 a12 write00100 read) Column
C00101 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q001011 q001012 q001013 q001014 q001015 q001016 q001017 q001018
a11 a12 write00101 read) Column
C00110 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q001101 q001102 q001103 q001104 q001105 q001106 q001107 q001108
a11 a12 write00110 read) Column
C00111 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q001111 q001112 q001113 q001114 q001115 q001116 q001117 q001118
a11 a12 write00111 read) Column
C01000 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q010001 q010002 q010003 q010004 q010005 q010006 q010007 q010008
a11 a12 write01000 read) Column
C01001 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q010011 q010012 q010013 q010014 q010015 q010016 q010017 q010018
a11 a12 write01001 read) Column
C01010 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q010101 q010102 q010103 q010104 q010105 q010106 q010107 q010108
a11 a12 write01010 read) Column
C01011 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30

WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q010111 q010112 q010113 q010114 q010115 q010116 q010117 q010118
a11 a12 write01011 read) Column
C01100 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q011001 q011002 q011003 q011004 q011005 q011006 q011007 q011008
a11 a12 write01100 read) Column
C01101 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q011011 q011012 q011013 q011014 q011015 q011016 q011017 q011018
a11 a12 write01101 read) Column
C01110 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q011101 q011102 q011103 q011104 q011105 q011106 q011107 q011108
a11 a12 write01110 read) Column
C01111 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q011111 q011112 q011113 q011114 q011115 q011116 q011117 q011118
a11 a12 write01111 read) Column
C10000 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q100001 q100002 q100003 q100004 q100005 q100006 q100007 q100008
a11 a12 write10000 read) Column
C10001 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q100011 q100012 q100013 q100014 q100015 q100016 q100017 q100018
a11 a12 write10001 read) Column
C10010 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q100101 q100102 q100103 q100104 q100105 q100106 q100107 q100108
a11 a12 write10010 read) Column
C10011 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q100111 q100112 q100113 q100114 q100115 q100116 q100117 q100118
a11 a12 write10011 read) Column
C10100 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q101001 q101002 q101003 q101004 q101005 q101006 q101007 q101008
a11 a12 write10100 read) Column
C10101 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0

d1 d2 d3 d4 d5 d6 d7 q101011 q101012 q101013 q101014 q101015 q101016 q101017 q101018
a11 a12 write10101 read) Column
C10110 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q101101 q101102 q101103 q101104 q101105 q101106 q101107 q101108
a11 a12 write10110 read) Column
C10111 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q101111 q101112 q101113 q101114 q101115 q101116 q101117 q101118
a11 a12 write10111 read) Column
C11000 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q110001 q110002 q110003 q110004 q110005 q110006 q110007 q110008
a11 a12 write11000 read) Column
C11001 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q110011 q110012 q110013 q110014 q110015 q110016 q110017 q110018
a11 a12 write11001 read) Column
C11010 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q110101 q110102 q110103 q110104 q110105 q110106 q110107 q110108
a11 a12 write11010 read) Column
C11011 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q110111 q110112 q110113 q110114 q110115 q110116 q110117 q110118
a11 a12 write11011 read) Column
C11100 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q111001 q111002 q111003 q111004 q111005 q111006 q111007 q111008
a11 a12 write11100 read) Column
C11101 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q111011 q111012 q111013 q111014 q111015 q111016 q111017 q111018
a11 a12 write11101 read) Column
C11110 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q111101 q111102 q111103 q111104 q111105 q111106 q111107 q111108
a11 a12 write11110 read) Column
C11111 (VDD VSS WL0 WL1 WL2 WL3 WL4 WL5 WL6 WL7 WL8 WL9 WL10 WL11 WL12 WL13
WL14 WL15 WL16 WL17 WL18 WL19 WL20 WL21 WL22 WL23 WL24 WL25 WL26 WL27 WL28 WL29 WL30
WL31 WL32 WL33 WL34 WL35 WL36 WL37 WL38 WL39 WL40 WL41 WL42 WL43 WL44 WL45 WL46 WL47
WL48 WL49 WL50 WL51 WL52 WL53 WL54 WL55 WL56 WL57 WL58 WL59 WL60 WL61 WL62 WL63 d0
d1 d2 d3 d4 d5 d6 d7 q111111 q111112 q111113 q111114 q111115 q111116 q111117 q111118
a11 a12 write11111 read) Column

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        // Output select muxes
        M1 (VDD VSS q000001 q000011 q000101 q000111 q001001 q001011 q001101 q001111
q010001 q010011 q010101 q010111 q011001 q011011 q011101 q011111 q100001 q100011
q100101 q100111 q101001 q101011 q101101 q101111 q110001 q110011 q110101 q110111
q111001 q111011 q111101 q111111 a6 a7 a8 a9 a10 q0) Mux32
        M2 (VDD VSS q000002 q000012 q000102 q000112 q001002 q001012 q001102 q001112
q010002 q010012 q010102 q010112 q011002 q011012 q011102 q011112 q100002 q100012
q100102 q100112 q101002 q101012 q101102 q101112 q110002 q110012 q110102 q110112
q111002 q111012 q111102 q111112 a6 a7 a8 a9 a10 q1) Mux32
        M3 (VDD VSS q000003 q000013 q000103 q000113 q001003 q001013 q001103 q001113
q010003 q010013 q010103 q010113 q011003 q011013 q011103 q011113 q100003 q100013
q100103 q100113 q101003 q101013 q101103 q101113 q110003 q110013 q110103 q110113
q111003 q111013 q111103 q111113 a6 a7 a8 a9 a10 q2) Mux32
        M4 (VDD VSS q000004 q000014 q000104 q000114 q001004 q001014 q001104 q001114
q010004 q010014 q010104 q010114 q011004 q011014 q011104 q011114 q100004 q100014
q100104 q100114 q101004 q101014 q101104 q101114 q110004 q110014 q110104 q110114
q111004 q111014 q111104 q111114 a6 a7 a8 a9 a10 q3) Mux32
        M5 (VDD VSS q000005 q000015 q000105 q000115 q001005 q001015 q001105 q001115
q010005 q010015 q010105 q010115 q011005 q011015 q011105 q011115 q100005 q100015
q100105 q100115 q101005 q101015 q101105 q101115 q110005 q110015 q110105 q110115
q111005 q111015 q111105 q111115 a6 a7 a8 a9 a10 q4) Mux32
        M6 (VDD VSS q000006 q000016 q000106 q000116 q001006 q001016 q001106 q001116
q010006 q010016 q010106 q010116 q011006 q011016 q011106 q011116 q100006 q100016
q100106 q100116 q101006 q101016 q101106 q101116 q110006 q110016 q110106 q110116
q111006 q111016 q111106 q111116 a6 a7 a8 a9 a10 q5) Mux32
        M7 (VDD VSS q000007 q000017 q000107 q000117 q001007 q001017 q001107 q001117
q010007 q010017 q010107 q010117 q011007 q011017 q011107 q011117 q100007 q100017
q100107 q100117 q101007 q101017 q101107 q101117 q110007 q110017 q110107 q110117
q111007 q111017 q111107 q111117 a6 a7 a8 a9 a10 q6) Mux32
        M8 (VDD VSS q000008 q000018 q000108 q000118 q001008 q001018 q001108 q001118
q010008 q010018 q010108 q010118 q011008 q011018 q011108 q011118 q100008 q100018
q100108 q100118 q101008 q101018 q101108 q101118 q110008 q110018 q110108 q110118
q111008 q111018 q111108 q111118 a6 a7 a8 a9 a10 q7) Mux32

ends Block
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